Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.106”**

**PAD FUNCTION:**

1. **OUT A**
2. **–IN A**
3. **+IN A**
4. **V+**
5. **+IN B**
6. **–IN B**
7. **OUT B**
8. **OUT C**
9. **–IN C**
10. **+IN C**
11. **V-**
12. **+IN D**
13. **–IN D**
14. **OUT D**

**2 1 14 13**

**12**

**11**

**10**

**3**

**4**

**5**

**6 7 8 9**

**1470W**

**MASK**

**REF**

**.163”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .005 x .005”**

**Backside Potential: V-**

**Mask Ref: 1470W**

**APPROVED BY: DK DIE SIZE .106” X .163” DATE: 10/22/19**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: OP470NBC**

**DG 10.1.2**

#### Rev B, 7/1